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and for Defendants AEROFLEX INCORPORATED, AMI SEMICONDUCTOR, INC., MATROX ELECTRONIC SYSTEMS, LTD., MATROX GRAPHICS, INC., MATROX INTERNATIONAL CORP. and MATROX TECH, INC.

UNITED STATES DISTRICT COURT

NORTHERN DISTRICT OF CALIFORNIA

SAN FRANCISCO DIVISION

RICOH COMPANY, LTD.,

Plaintiff,

vs.

AEROFLEX INCORPORATED, et al.,

Defendants.

SYNOPSYS, INC.,

Plaintiff,

vs.

RICOH COMPANY, LTD., a Japanese corporation

Defendant.

Case No. C03-04669 MJJ (EMC)

Case No. C03-2289 MJJ (EMC)

SYNOPSYS, INC.'S AND AEROFLEX INC. ET AL.'S PROPOSED DEFINITIONS FOR THE TEN TERMS IDENTIFIED FOR CONSTRUCTION AT THE CLAIM CONSTRUCTION HEARING

Date: December 15, 2004
Time: 2:30 PM
Courtroom: 11
Judge: Martin J. Jenkins

Pursuant to the Amended Order of the Court dated November 30, 2004, Plaintiff Synopsys, Inc. ("Synopsys") and Defendants Aeroflex Incorporated, AMI Semiconductor, Inc., Matrox Electronic Systems, Ltd., Matrox Graphics, Inc., Matrox International Corp. and Matrox Tech, Inc. (collectively, "Aeroflex, et al.") submit the following proposed definitions of the ten terms, phrases and clauses for construction at the Claims Construction hearing now set for December 15, 2004, at 2:30 p.m.

Term	**Proposed Definition**	**Supporting Intrinsic Evidence**
8 A computer-aided design process for designing	a process that uses a computer for designing, as distinguished from a computer-aided manufacturing process, which uses a computer to direct and control the manufacturing process.	**'432 patent**: 1:9-12, 16:34-65 **Cross-reference to brief**: §V.A (pp. 24-26)
1 Architecture independent actions and conditions	the logical steps and decisions that are represented as rectangles and diamonds in the flowchart; where register-transfer level (RTL, as defined in Darringer et al.) descriptions are excluded. An RTL description defines any control needed for the ASIC and consists of: 1) defining the inputs, outputs, and any registers of the proposed ASIC; and, 2) describing for a single clock cycle of the ASIC how the ASIC outputs and any registers are set according to the values of the ASIC inputs and the previous values of the registers.	**432 patent:** 2:24-27; 3:49-59; 4:15-19; 4:61-63; 6:3-14; 7:20-23; 8:47-51; 16:34-65 **'432 patent file history** April 1989 Amendment at 8-11, 13; October 1989 Examiner Interview Summary; November 1989 Amendment at 6-7. **'435 patent (Darringer et al.):** Fig.4; 4:26-32; 5:27-35 **Cross-reference to brief**: §V.C.1 & §V.C.3 (pp. 27-31, 34-38).
3 Describing . . . a series of architecture independent actions and conditions	the designer represents a sequence of logical steps (rectangles) and decisions (diamonds), and the transitions (lines with arrows) between them in a flowchart format that excludes any register-transfer level (RTL, as defined in Darringer et al.) descriptions	**'432 patent**; Figs. 1a, 5, and 7, 2:21-27, 3:20-22, 3:50-59, 4:5-22, 4:35-38, 7:12-23, 16:34-65 **'432 patent file history**: April 1989 Amendment at 9, 11; October 1989 Examiner Interview Summary; November 1989 Amendment at 6-7 **'016 patent**; 7:33-9:52 **'435 patent (Darringer et al.):** 4:26-33 Cross-reference to brief: §V.C.1 (pp.

Term	Proposed Definition	Supporting Intrinsic Evidence
		27-31)
2 specifying for each described action and condition of the series one of said stored definitions	the designer assigns one definition from the set of stored definitions for each of the described logical steps and decisions represented in the flowchart	**'432 patent**; Fig. 5, 3:20-22, 4:61-63, 5:20-22, 7:24-25, 8:23-26, 8:51-56, 16:34-65 **'016 patent**; 6:12-32 **Cross-reference to brief**: §V.C.2 (pp. 31-33)
9 A set of definitions of architecture independent actions and conditions	a set of named descriptions defining the functionality and arguments for the available logical steps and decisions that may be specified in the flowchart where register-transfer level (RTL, as defined in Darringer et al.) descriptions are excluded.	**432 patent:** 2:24-27; 3:49-59; 4:15-19; 4:61-63; 5:20-22; 6:3-14; 7:20-50; 8:47-51; 16:34-65 **'432 patent file history** April 1989 Amendment at 8-11, 13; October 1989 Examiner Interview Summary; November 1989 Amendment at 6-7. **'435 patent (Darringer et al.):** Fig.4; 4:26-32; 5:27-35 **Cross-reference to brief**: §V.C (pp. 27-38)
10 Selecting from said stored data for each of the specified definitions a corresponding integrated circuit hardware cell	mapping the specified stored definitions for each logical step and decision represented in the flowchart to a corresponding stored hardware cell description.	**'432 patent**: Fig. 4, 3:16-19, 4:66-5:3, 5:22-29, 8:31-37, 8:58-60, 9:52-60, 16:34-65 **'432 patent file history**: April 1989 Amendment at 10 **Cross-reference to brief**: §V.E.1 (pp. 41-44)
4 Said step of selecting a hardware cell comprising applying to the specified definition of the action or condition to be performed	the mapping of the specified definitions to the stored hardware cell descriptions must be performed by applying to the specified definitions in the flowchart a set of cell selection rules stored in an expert system knowledge base	**'432 patent**: Abstract, 2:58-63, 5:6-8, 8:29-37, 8:58-60, 9:8-13, 11:16-26, 16:34-65 **'432 patent file history**: April 1989 Amendment at 8-11, 17; October 1989 Examiner Interview Summary; November 1989 Amendment at 4, 6-7, 9 **'435 patent (Darringer):** 7:32-9:35 '**603 patent**: 3:59-63 **An Overview of Logic Synthesis Systems**: at 170 **The CMU Design Automation**

Term	Proposed Definition	Supporting Intrinsic Evidence
		System: at 75-77 **'016 patent**: 3:5-8, 9:67-10:2 **Cross-reference to brief**: §V.E.1 (pp. 41-44)
5 A set of cell selection rules	a set of rules embodying the knowledge of expert designers for application specific integrated circuits, each rule having an antecedent portion (e.g., IF) and a consequent portion (e.g., THEN), which enables the expert system to map the specified stored definitions for each logical step and decision represented in the flowchart to a corresponding stored hardware cell description	**'432 patent**: 2:58-63, 8:20-30, 8:58-9:62, 10:39-11:26, 14:50-59, 15:53-58, 16:34-65 **'432 patent file history**: April 1989 Amendment at 9-11, 15, 17; October 1989 Examiner Interview Summary; November 1989 Amendment at 7, 9 **'435 patent (Darringer)**: 7:32-9:35 **An Overview of Logic Synthesis Systems**: at 170 **The CMU Design Automation System**: at 75-77 **Cross-reference to brief**: §V.E.3 (pp. 47-49)
6 Expert system knowledge base	the knowledge base portion of an expert system software having a set of rules, each rule having an antecedent portion (e.g., IF) and a consequent portion (e.g., THEN), and embodying the knowledge of expert designers for application specific integrated circuits. An expert system is software that solves problems through selective application of the rules in the knowledge base by an inference engine, as distinguished from conventional software, which uses a predefined step-by-step procedure (algorithm) to solve problems.	**'432 patent**: 2:58-63, 5:6-8, 8:29-37, 8:58-60, 9:8-13, 11: 16-26, 16:34-65 **'432 patent file history**: April 1989 Amendment at 8-11, 17; October 1989 Examiner Interview Summary; November 1989 Amendment at 4, 6-7, 9 **'435 patent (Darringer)**: 7:32-9:35 **'603 patent**: 3:59-63 **An Overview of Logic Synthesis Systems**: at 170 **The CMU Design Automation System**: at 75-77 **'016 patent**: 3:5-8, 9:67-10:2 **Cross-reference to brief**: §V.E.2 (pp. 44-47)

Term	Proposed Definition	Supporting Intrinsic Evidence
7 A netlist defining the hardware cells which are needed to perform the desired function of the integrated circuit	producing a list of the needed hardware cells by eliminating any mapped hardware cells that are redundant or otherwise unnecessary, producing a custom controller type hardware cell for providing the needed control for those other hardware cells, and producing the necessary structural control paths and data paths for the needed hardware cells and the custom controller	**'432 patent**: Abstract, 1:17-37, 2:39-44, 4:39-43, 5:8-12, 5:30-40, 9:62-10:9, 13:55-14:3, 16:34-65 **Cross-reference to brief**: §§V.F.1 and V.F.3 (pp. 49-50, 51-52)

Dated: December 2, 2004

Respectfully submitted,

HOWREY SIMON ARNOLD & WHITE, LLP

By: /s/ Thomas C. Mavrakakis
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